Saurabh Dutta Chowdhury

155 24 th Avenue #4 San Francisco, CA 94121

(650) 492 0712

Sdchowdhury@alumni.harvard.edu

WORK EXPERIENCE

2021-Present	Power Integrations San Jose, CA: Sr Staff Technology Development GaN Foundry
2011-20	Transphorm Goleta, CA: Sr Director GaN Foundry
2004-2011	Maxim Integrated Products San Jose, CA: Manager Process Engineering-Plasma
2000-2004	Cypress Semiconductor San Jose CA: Principal Engineer Plasma Etch
1995-2000	Applied Materials Santa Clara, CA Sr Process Engineer Plasma Etch

EDUCATION

Strategic Studies

PhD in Defense Studies at King's College London Granted in 2016
Thesis Topic: Indian Nuclear Testing Decisions: A Foreign Policy Analysis Framework based Model Supervisors: Dr. Harsh Pant & Dr. Wyn Bowen

MA, Monterey Institute of International Studies-Middlebury
2010 Nonproliferation Studies

Management Studies

Program for Leader Development (PLD) -Harvard Business School 2006-07 Sponsored by Employer-Maxim Integrated Products

MBA Santa Clara University-Concentration Finance
1998 -2001 Sponsored by Applied Materials

IC Processing Studies

MEng, Rochester Institute of Technology
Microelectronics Engineering 1994
(Sematch/SRC Fellowship)

UG Studies

The University of the South-Sewanee, USA
BS (Cum Laude) Physics and Math 1993
(Full Academic Scholarship-entire time)

PUBLICATIONS

IEEE Technical GaN Foundry

650 V Highly Reliable GaN HEMTs on Si Substrates over multiple generations: Expanding usage of a mature 150 mm Si Foundry (2019 30th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC) Saratoga Springs 2019)

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5000+ Wafers of 650 V Highly Reliable GaN HEMTs on Si Substrates: Wafer Breakage and Backside Contamination Results (2020 31st Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC) Saratoga Springs 2020)
Published IEEE Transactions in Semiconductor Manufacturing-2020

650 V Highly Reliable GaN HEMTs on Si Substrates over Multiple Generations: Matching Silicon CMOS Manufacturing Metrics and Process Control (2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)**, Austin TX)**

600 V JEDEC-qualified highly reliable GaN HEMTs on Si substrates
2014 IEEE International Electron Devices Meeting, San Francisco, CA

SPIE Technical Silicon Foundry

Line-edge roughness reduction for advanced metal gate etch with 193-nm lithography in a silicon decoupled plasma source etcher (DPSII) (Proc. SPIE 5039, Advances in Resist Technology and Processing XX, (12 June 2003))

Gate Etch Process Control (Proc. SPIE 5038, Metrology, Inspection, and Process Control for Microlithography XVII, (2 June 2003);

Gate Etch CD control using MIMO FutureFab 2004 ,SPIE2004

Photolithography Process Characterization using Development Rate Monitor
(SPIE Microlithography, Advances in Resist Technology 1995)

Aluminum DualDamascene: IITC Conference May1999,Burlingame,CA.

AVS Technical Silicon Foundry

Multilayer Gate Stack for line edge roughness reduction in 193nmlithography U.S. Patent Number 7,229,929

PATENTS

Insitu hardmask approach for self-aligned contact etch US Patent 7,078,334

Borderless Contact Architecture US Patent 6713831

Method for forming subcritical dimension structures in an integrated circuit US

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Patent 662715

AFFILIATIONS

Semiconductors

Member IEEE

Member Technical Committee SEMI

Dean's Advisory Council: Dept of Microelectronics Engineering at Rochester Inst of Technology, Rochester, NY USA

STRATEGIC STUDIES

Journal Paper

A Two Variable Proliferation Model: Implications for US Policy towards Iran(Accepted for Publication in the Winter 2013 edition of Nuclear Notes-CSIS)

STRATEGIC STUDIES CONFERENCE PAPERS

Prospects for Indo-Japan Nuclear Cooperation: A Synthetic Foreign Policy Analysis based Framework (Accepted for invited talk at Kyoto University February 2015)

Indian Nuclear Testing Decision Making: A Foreign Policy Analysis framework based model (Accepted for Young Scholars Program at ISA West Sept 2014)

Indian Nuclear Testing Decision Making: A Foreign Policy Analysis framework based model (Accepted for Presentation: ISA FLASCO Buenos Aires)

Indian Nuclear Testing and Non-testing decisions: Mapping nine cases since latency to explain dominant causal mechanisms (Accepted for Presentation at ISA-ISSS Conference 2013 to be held at George Washington University Oct 4-6)

STRATEGIC STUDIES

Engaging the Scientific Enclave in India towards Nonproliferation post Indo-US Civil nuclear agreement (PONI Conference Proceedings 2010. CSIS)

AWARDS

Essay "The Indian Nuclear Testing Puzzle: Bureaucratic Politics Models and Implications for Future US Nonproliferation Policy" selected as one of five finalist of the 2012 Doreen & Jim McElvany Nonproliferation Challenge Center for Nonproliferation Studies -Monterey

Honorary Post Doc University of Leicester 2020 working on publication of PhD thesis into Book to be published by Routledge South Asia Series under guidance

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from PhD External Examiner-Dr Andrew Futter (Univ of Leicester UK)

Member Aurndel House Library at IISS London

STRATEGIC STUDIES WORKSHOP

Indo-US Nuclear Dialog with Jawaharlal Nehru University students(CSIS 2010) Nuclear Workshop (Institute for Peace and Conflict Studies New Delhi) 2011 CTBTO Public Diplomacy Course in Vienna in July 2013

QUANTITATIVE

ISA Workshop: Nuclear Politics Beyond Positivism in April 2013 at San Francisco

Experience

Regression Analysis, Bayesian Statistics, Likelihood estimation. JMP/SAS

TEACHING

Experience

Teaching Assistant for Finite Math 104 at The University of the South Summer 1992

Teaching Assistant , RIT Learning Lab 1993-94
Taught Underprivileged inner city students from the Bronx and Brooklyn on a bootcamp in RIT in Summer of 1994

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REFERENCES

Dr Umesh Misra Founder Transphorm, University of California Santa Barbara

GAN/SEMI

Yoshimuri Asai, Aizu Fujitsu Semiconductor Wafers Ltd (AFSW)

Dr. Peter Smith, Device Technologist Transphorm Goleta, CA

Dr. Rakesh Lal, Device Technologist Transphorm Goleta, CA

Dr. Amitava Das, CEO Tagore Technologies, Arlington Heights, IL

Dr. Shahin Sharifzadeh,Co- CEO NextGen Power Systems, San Jose, CA (Supervisor at Cypress from 2000-2004)

Vijay Ullal, Venture Capitalist Saratoga CA (Supervisor Maxim Integrated Products San Jose from 2004-11)

Mr. Gopal Krishna ex MD Maxim India Bengaluru in the context of Maxim Gandhinagar which was scaled up by me from 2007-09.

Dr JB Price, Supervisor Los Gatos, CA Supervisor at Applied Materials-1995-2000

Ajit Manocha, President SEMI Milpitas, CA

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STRATEGIC

Studies

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